Synopsis V1.0
HI SEE Test Report for the STMicroelectronics 1G NAND Flash Memory

Tim Oldham, Perot Systems Government Services, Inc. /NASA-GSFC
Jim Howard, MEI Technology Inc./NASA-GSFC
Ray Ladbury, NASA GSFC
Hak Kim, MEI Technology Inc./NASA-GSFC
Mark Friendlich, MEI Technology Inc./NASA-GSFC
Melanie Berg, MEI Technology Inc./NASA-GSFC

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I. Introduction

This study was undertaken to determine the susceptibility of the STMicroelectronics NAND01GW3B2ANGE 1 Gbit NAND Flash memory to destructive and nondestructive single-event effects (SEE). The device was monitored for SEUs and for destructive events induced by exposing it to a heavy ion beam at the Lawrence Berkeley National Laboratory Cyclotron facility, and at the Texas A&M University Cyclotron.

II. Devices Tested

We tested a total of 2 STMicroelectronics NAND01GW3B2ANGE 1G NAND devices marked with date code 0604. Note that with commercial devices, the same lot date code is no guarantee that the devices are from the same wafer diffusion lot or even from the same fabrication facility.

The device technology is 90 nm minimum feature size CMOS NAND Flash memory. The chips came in a 48-pin TSOP package, but the plastic had been dissolved on the topside to expose the chips, allowing the beam to reach the chip surface.

Fig. 1. Photo of die

III. Test Facilities

Facility: Lawrence Berkeley National Laboratory Cyclotron
Flux: (5 x 10^3 to 1. x 10^5 particles/cm^2/s).
Fluence: All tests were run to 1E5 to 1E8 p/cm^2, or until destructive or functional events occurred.

Facility: Texas A&M University Cyclotron
Flux: (5 x 10^3 to 1. x 10^5 particles/cm^2/s).
Fluence: All tests were run to 1E5 to 1E8 p/cm^2, or until destructive or functional events occurred.

Table I: Ions/Energies and LET for this test

LBNL Ions	Energy/ AMU	Energy (MeV)	Approx. LET on die (MeV•cm^2/mg)	Angle	Effective LET
Ne	4.5	90	3.49	0	3.49
Ar	4.5	180	9.47	0	9.47
Cu	4.5	284	21.0	0	21
Kr	4.5	378	30.85	0	30.85
Xe	4.5	581	58.7	0	58.7
TAMU Ions	**Energy/ AMU**	**Energy (MeV)**	**LET (MeV-cm^2/mg)**	**Angle**	**Effective LET**
Ne	40	800	1.2	0, 60	1.2, 2.4
Ar	40	1600	3.9	0	3.9

IV. Test Conditions

Test Temperature: Room Temperature for SEU
Operating Frequency: (0-30 MHz).
Power Supply Voltage: (3.3V and 3.3V-10% for SEU).

V. Test Methods

Because Flash technology uses different voltages and circuitry depending on the operation being performed, testing was performed for a variety of test patterns and bias and operating conditions.

Test patterns included all 0's, all 1's, checkerboard and inverse checkerboard. In general all these patterns were used until a worst-case pattern was established, and then testing was conducted using only the worst-case pattern. Between exposures, all patterns were used to exercise the DUT, to verify that it was still fully functional. The maximum clock frequency for these devices was 30 MHz, which is also the frequency used in the dynamic testing.

Bias and operating conditions included:

1) Static/Unbiased irradiation, in which a pattern was written and verified, and then bias was removed from the part and the part was irradiated. Once the irradiation reached the desired fluence, it was stopped, bias was restored, and the memory contents were read and errors tallied.

2) Static irradiation, which was similar to unbiased irradiation, except that bias was maintained throughout irradiation of the part.

Note that these conditions provide no opportunity to monitor functional or hard failures that may occur during the irradiation.

3) Dynamic Read, in which a pattern was written to memory and verified, then subsequently read continuously during irradiation. This condition allows determination of functional, configuration and hard errors, as well as bit errors.

4) Dynamic Read/Write, which was similar to the Dynamic Read, except that a write operation is performed on each word found to be in error during the previous Read.

5) Dynamic Read/Erase/Write, which again was similar to the Dynamic Read and Read/Write, except that a word in error was first erased and then rewritten. Because the Erase and Write operations use the charge pump, it is expected that the Flash could be more vulnerable to destructive conditions during these operations.

6) It was also intended to conduct latchup testing at 70° C, and 3.6 V, but the heating element did not work, so all testing was done at room temperature. The DUTs were monitored for latchup in the tests actually conducted, but this is not a realistic worst-case test condition.

The Block diagram for control of the DUT is shown in Figure 2. The FPGA based controller interfaces to the FLASH daughter card and to a laptop, allowing control of the FPGA and uploading of new FPGA configurations and instructions for control of the DUT. Power for the flash is supplied by means of a computer-controlled power supply. The National Instruments Labview interface monitors the power supply for over-current conditions and shuts down power to the DUT if such conditions are detected.

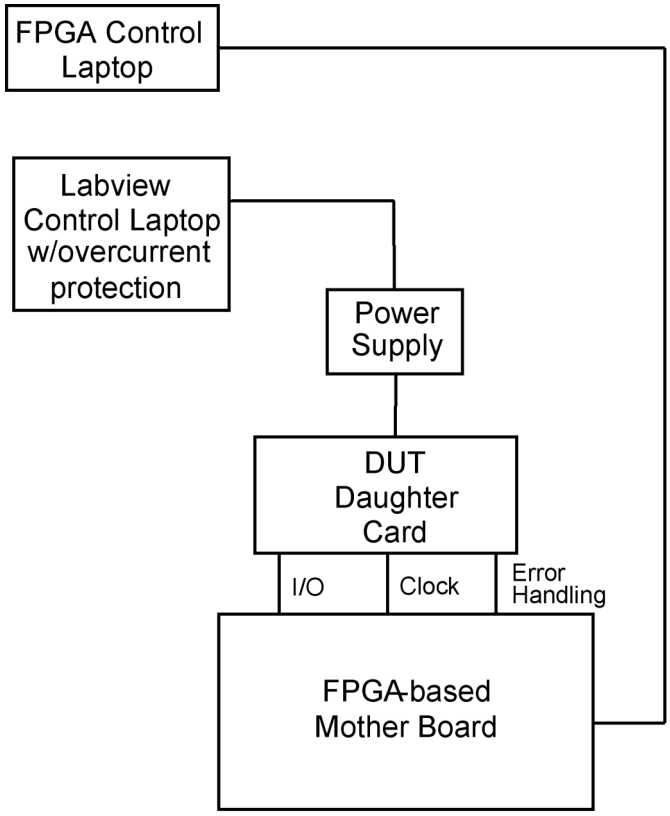
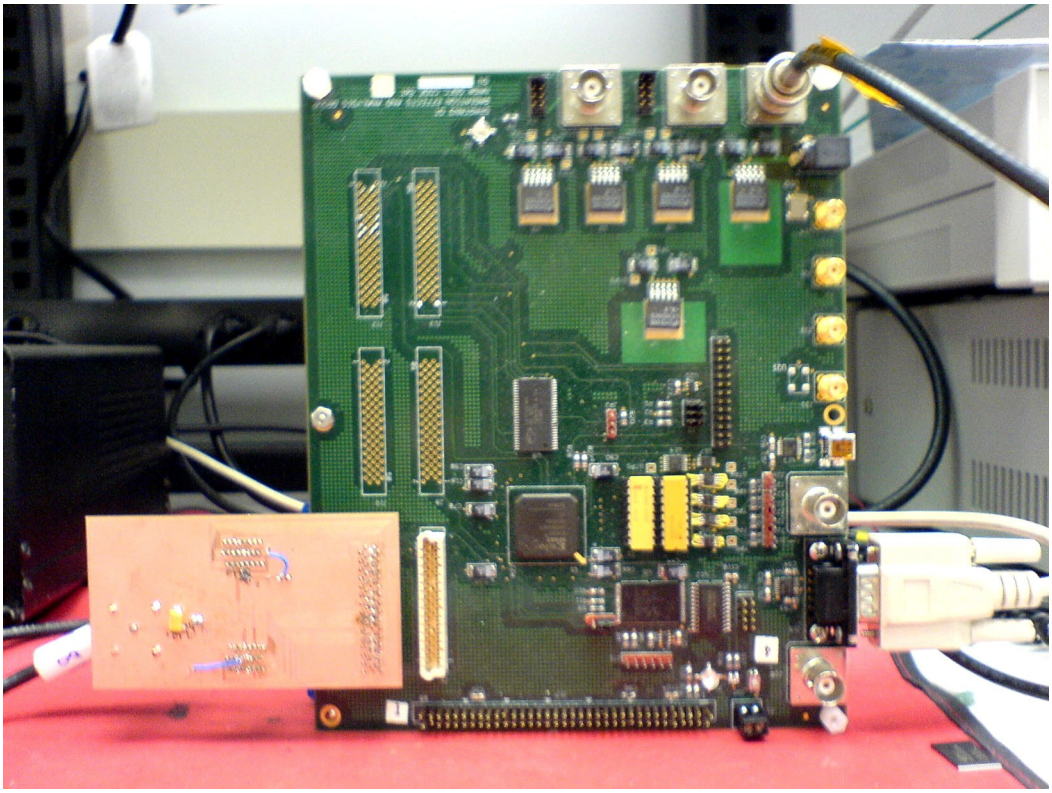
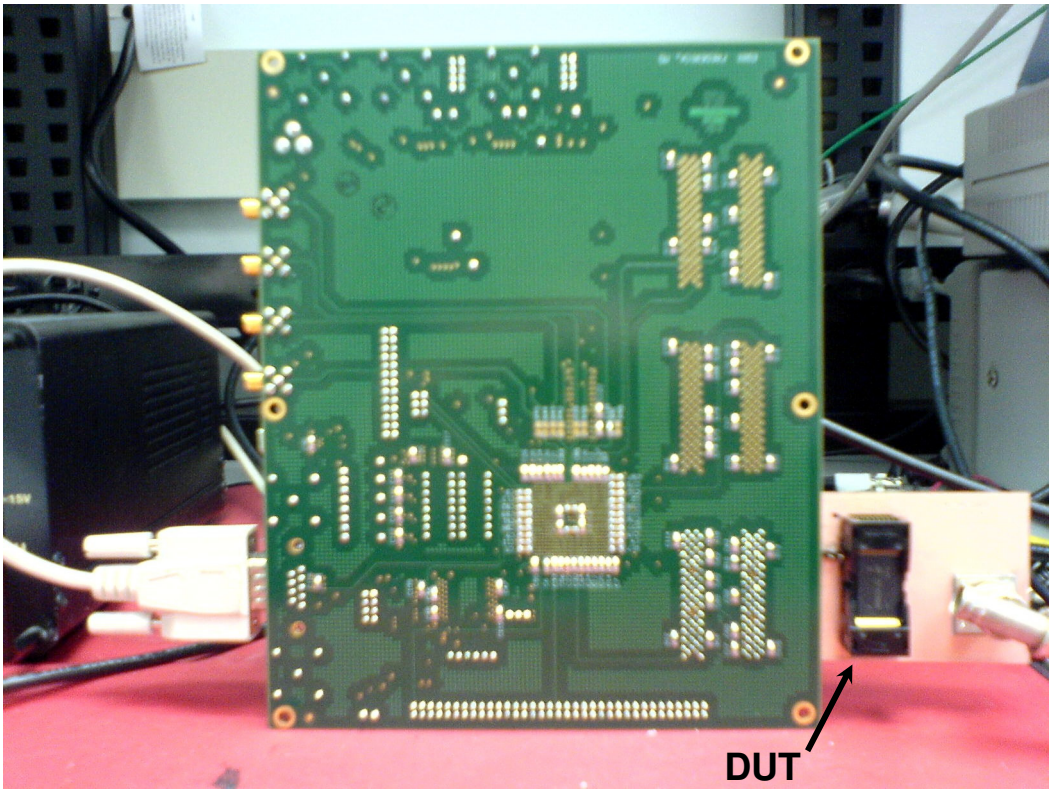


Figure 2. Overall Block Diagram for the testing of the STMicroelctronics NAND Flash.



(a)



(b)

Fig. 3. Pictures of test board. (a) front of mother board, (b) front of daughter board, showing DUT.

VI. Results

During testing, the NAND01GW3B2ANGE was irradiated with the ions indicated in Table I. The DUT was oriented normal to the incident beam, except as noted. The errors observed in static testing are shown in Fig. 4.

Even for the static case, bit errors and Page/Block errors were evident in the patterns of upsets observed. It is likely that the Page/Block errors arise due to upsets in configuration registers in the memory array. Because the DUT was not actively exercised during the exposure, we could not determine exactly when a page/block error occurred, so cross sections are approximate for these error modes. Here and in the following discussion, bit errors are taken to be single bits, which are flipped, as a result of the interaction with incident ions, normally from zero to one. We do not have the physical to logical address mapping, which would allow us to look for multiple bit errors (error clusters) for these parts. However, in the overwhelming majority of cases, there is only one error in a page, or one error in an entire block, which makes it extremely unlikely that there will be multiple errors from a single ion. This result is consistent with previously published results on the upset mechanism in flash memory—an ion passing through a floating gate creates a dense charge column, which creates a conducting path between the gate and substrate, which allows charge to leak off the floating gate. Since the ion only hits one gate, only one bit is affected. This situation is far different from that in volatile memories, where charge generated in the Si substrate can be shared across multiple nodes. The only apparent multiple bit errors are cases where an entire page or a block (or a large part of one) upsets simultaneously—these page and block errors are attributed to errors in the control logic, rather than to the individual bits. These are counted as SEFIs (Single Event Functional Interrupt). In general, a SEFI is any event where the entire DUT, or a large part of it, stops working, presumably from an interaction with a single ion. As a practical matter, most of the SEFIs recorded here are either page errors or block errors, although a few involve multiple pages or multiple blocks. Some are also watchdog errors, where the DUT simply stopped responding to commands.

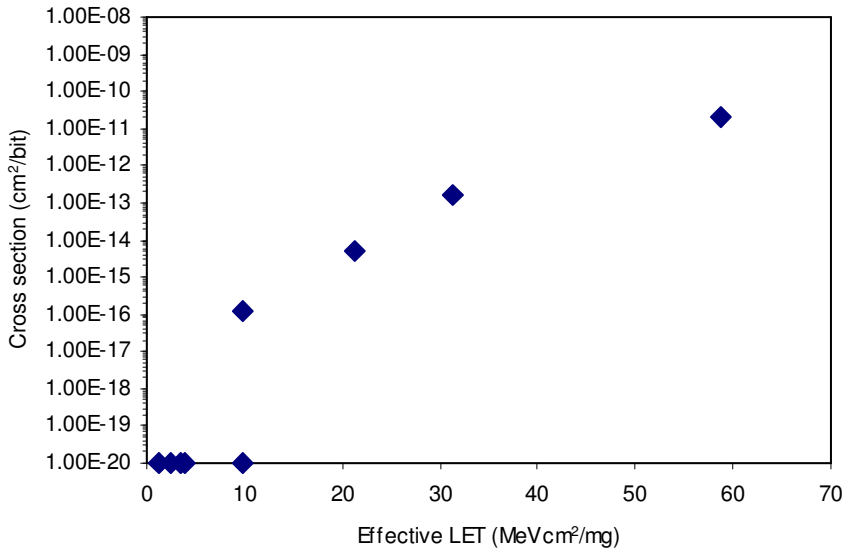


Fig. 4. Error cross-sections observed in static testing.

The results in Fig. 4 were fitted with Weibull parameters, threshold LET=9.74, saturation cross section=1.15E-11 cm^2/bit, width=48, exponent=5, and Creme96 was used to calculate the bit error rate for geosynchronous orbit at solar minimum. The result was 1E-12 errors/bit-day, which is equivalent to about 0.4 bit errors per year for a 1G. The data in Fig. 4 is replotted in Fig. 5, normalized per device, instead of per bit, so that the SEFI effects can be shown on the same scale. In this case, the only SEFI was an increase in power supply current, which required a DUT reset. Obviously, the SEFI error cross sections are much less than the bit upset cross section, and the error rate expected in space will scale with the cross section. However, we have not calculated this error rate, because there are so few SEFI events that there is large statistical uncertainty associated with them. However, we note that the Creme96 input spectrum indicates only about $1.4x10^{-4}$ particles/cm^2-sr-sec at the LET where the one SEFI was observed, or higher. This is equivalent to about one particle/cm^2 every 20 years. For this reason, one would expect the SEFI rate to be manageable, in the static operating mode.

For the Dynamic Read condition, the parts showed exhibited transient read errors in addition to the bit and Page/Block errors, and other SEFIs, which are plotted in Fig. 6. For Ne and Ar ions (LET up to 9.74), there were no static bit errors at any LET, detected after the beam was turned off. There were transient read errors, as shown in Fig. 6, at these LETs, which are thought to be due to noise in the read circuit. At higher LETs (Cu, Kr, and Xe ions), SEFIs were observed on all shots, which made it difficult to count the transient errors—if the DUT stops responding to commands, it is hard to say what errors were not counted. After the DUT was restored to operating condition, it could still be checked for static bit errors, however. These results are shown in Fig. 6. In Fig. 6, we have attempted to count SEFI events, despite the obvious difficulties of doing so. For example, one can count block errors, but it is often unclear whether these are independent events or not. We have assumed that block or page errors at widely separated addresses are independent events, and block or page errors at consecutive addresses are one event. Of course, if the DUT stops responding to commands, there may be other events that were missed completely. The number of SEFI events is small in any case. As always, the statistical uncertainty associated with rare events is large.

Results of the dynamic R/W tests are shown in Fig. 7. Generally these results are unremarkable, because the usual zero-to-one errors are rewritten as they occur. For this reason, there are fewer errors indicated than in Fig. 6. The main reason for including this test was the expectation that the high voltage write operation would contribute to more errors in the control circuits, but this appears not to have happened, at least not on a large scale. Probably, this is because the write operation is performed only when a one to zero error is detected. For this circuit, one thousand such errors are still only one part per million of the entire memory, so the write circuit duty cycle is a very small number. Where a static cross section is given, it is based on the number of errors detected after the exposure and resetting of the DUT. The transient cross section is based on errors detected during the exposure. But some of the transient errors are probably really static bit errors that were rewritten during the test.

Results for the dynamic R/E/W tests are shown in Fig. 8, to the extent that they can be determined. For this condition, there were many more SEFIs than in the R/W (without erase) mode, which is probably due to the fact that every block is erased and rewritten on every cycle, so that the duty cycle for high voltage operations is much higher. As a practical matter, there are many page and block errors, which usually appear to be independent, on every shot with LET at or above 9.74 (Ar). With many large chunks of the memory completely knocked out, it becomes impossible to determine static or transient errors affecting only single bits.

All the testing was done at room temperature, which is not a worst-case condition for SEL (single event latchup). However, we did monitor the DUTs for SEL, but no true SEL was observed. The DUTs typically drew about 3 mA prior to turning on the beam, which often fluctuated during the exposure. On every exposure that resulted in a SEFI, the current would increase to 8 or 15 or even 30 mA, before dropping back to 3 mA, and this might happen several times. We take these results to indicate bus contention, rather than latchup, because a generalized latchup condition would not be expected to correct itself, without power cycling. A representative result is illustrated in Fig. 9.

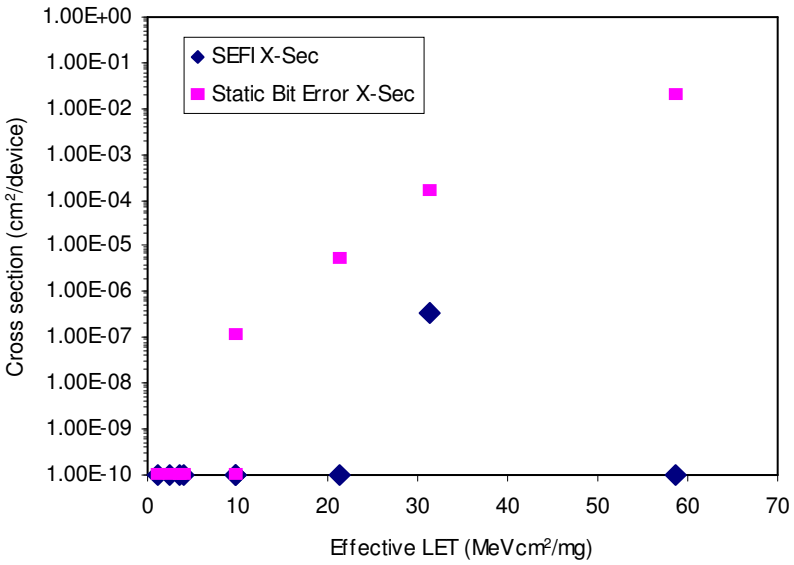


Fig. 5. Static upset cross sections.

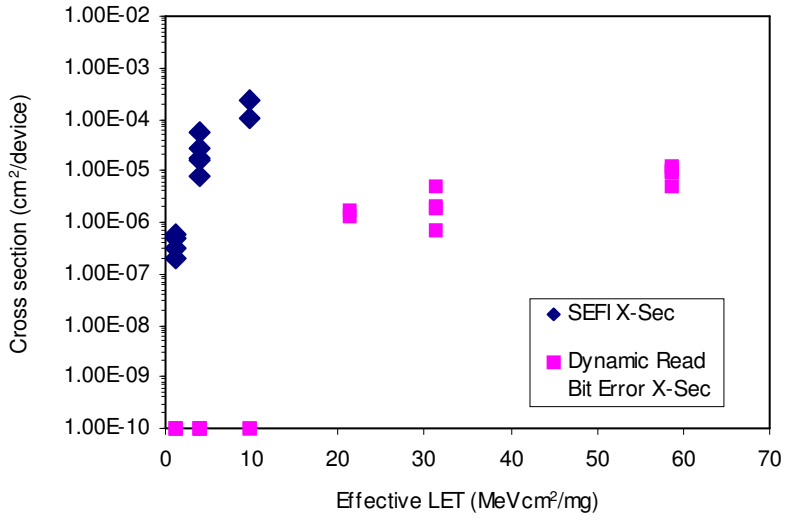


Fig. 6. Dynamic read upset cross section.

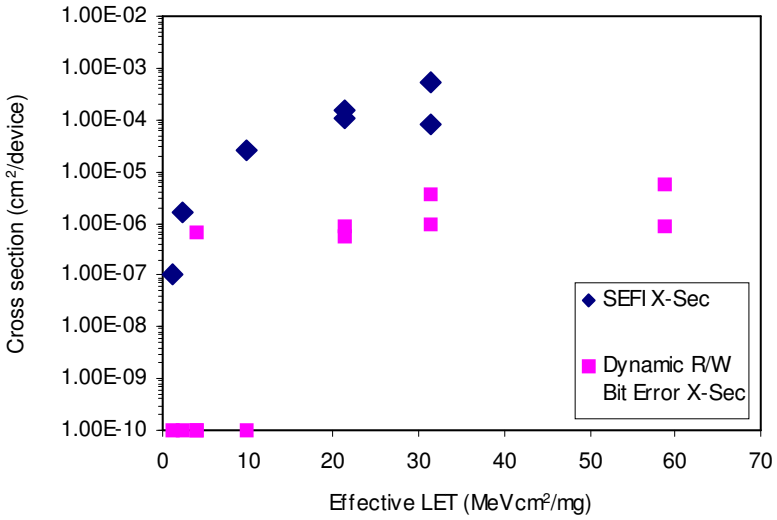


Fig. 7. Error cross sections observed in dynamic read/write testing.

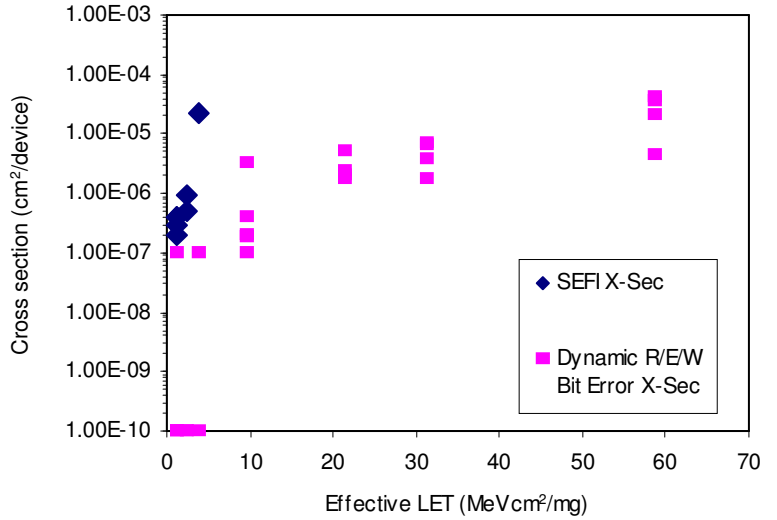


Fig. 8. Error cross sections observed in dynamic Read/Write/Erase testing.

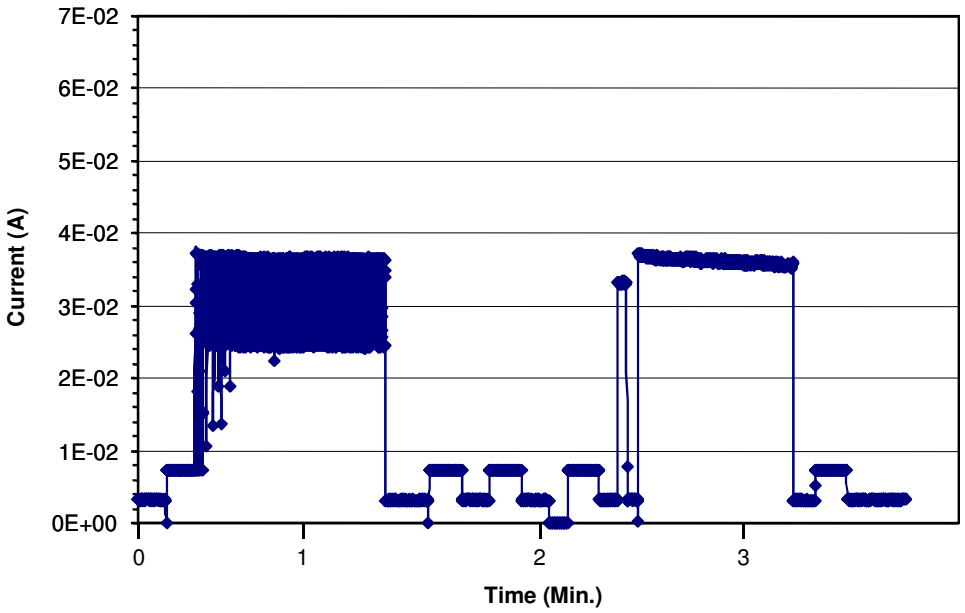


Fig. 9. Current vs Time, no latchup.

VII. Recommendations

The STMicroelectronics NAND01GW3B2ANGE 1-Gbit NAND Flash memory has TID tolerance above 30 krad (SiO_2), as reported previously, which is less than is usually desired for NASA missions, but it may be acceptable in specific cases. The static bit error rate, reported here, is low enough to make the technology very attractive for some NASA missions. However, SEFIs were observed on every shot above modest LETs, which will require mitigation strategies that have not been worked out yet. Whether or not the technology is suitable for a specific mission depends on the mission requirements.

VIII. Further Test Requirements

This test represents a preliminary characterization of SEE vulnerability of the STMicroelectronics NAND01GW3B2ANGE 1-Gbit. Although the static bit error rate is projected to be very good in space, additional testing is required before these devices can be considered for space applications. In particular, SEFIs will need to be better understood, and mitigation strategies identified.

In prior TID testing, these devices showed some promise for applications with moderate dose levels. Additional TID testing is recommended to fully characterize TID degradation, especially at low dose rates characteristic of space environments.